**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** (for administrative use)

**ISSUE TITLE:** [Pin Reference]

**REQUESTOR:**  Walter Katz, Signal Integrity Software, Inc.

**DATE SUBMITTED:** (Draft 3\_ross, May 17, 2016)

**DATE REVISED:** (for administrative use)

**DATE ACCEPTED:** (for administrative use)

**DEFINITION OF THE ISSUE:**

All measurements (“IBIS Data”) that are used to generate voltage values for IBIS subparameters within the [Model], [Model Spec], [Submodel Spec], and [Receiver Thresholds] keywords and are relative to a test fixture reference node or a simulator reference node.

IBIS defines the derivation of “IBIS Data” consisting of I-V, V-T, ISSO and voltage thresholds for a device under test. For I-V, voltages are defined as measured across the associated [Pullup], [Pulldown], [POWER Clamp], and [GND Clamp] elements. For V-T, ISSO and voltage thresholds, IBIS defines the reference node used to measure these voltages. IBIS contemplates the use of these models with the buffer supplied by specific rail voltages prescribed by the [Voltage Range], [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], [GND Clamp Reference], and [External Reference] (“[\*\*\* Reference]”) keywords. These voltages are measured relative to the test fixture reference.

During a simulation that uses IBIS Models, the IBIS specification is not clear what node should be used as the reference node for these voltages. This is not an issue when the simulator supplies rail voltages (“\*\*\*\_ref”) to a model relative to the simulator reference node that are same as the reference voltages (“[\*\*\* Reference]”) supplied to the buffer when generating the IBIS Data. Some EDA tools use the terminal of the IBIS model that has a [\*\*\* Reference]=0.0V as the reference node for measurements. As a result, when a model is simulated with voltages applied to the models' rail terminals (relative to a EDA tool reference node) other than the prescribed values, it is not defined in the specification how to compare the voltages at the buffer I/O (pin) terminal with the thresholds that were generated relative to the test fixture reference.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Allow an EDA tool to use IBIS model threshold in simulations where the voltages applied to a model rail terminals are not the same as the voltages applied to the rail terminals of the model when the “IBIS Data” is generated.
 |  |
|  |  |

(Enumerate each requirement in the table above, adding rows as needed.)

**SUMMARY OF PROPOSED CHANGES:**

This BIRD address this confusion by specifying supply pinwhose voltage the EDA tool can use to adjust the voltage measurement at the model I/O terminal that can be compared with the model thresholds.

For review purposes, the proposed changes are summarized as follows:

Table 2: IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| New [Component] section [Pin Reference] keyword | New | It is requiredthat there is a [Pin Mapping] section in the [Component]  |

**PROPOSED CHANGES:**

**Add to section 5 after [Pin Mapping]:**

*Keyword:* **[Pin Reference]**

*Required:* No

*Description:* This keyword defines for an I/O pin\_name under the [Pin] keyword a bus\_label entry to be used as reference node for voltage measurements at the I/O pin.

*Sub-Params:* bus\_label

*Usage Rules:* For each pin\_name listed, the simulation node at the bus\_label shall be used as the reference node of measurements at the pin\_name node when comparing simulation results with model thresholds.

The [Pin Reference] keyword is followed by the column heading bus\_label. Under the [Pin Reference] keyword each line of data consists of two columns for the pin\_name entry and bus\_label entry. Each pin\_name pin must exist under the [Pin] keyword.

Only pin\_name pins that are for Input\*, Output\*, or I/O\* models described later under Model\_type need to be listed. However, the listing of any pin\_name is optional.

The [Pin Mapping] keyword, where bus\_label entries are defined, must exist.

\*\* (Additional rules already exits in [Pin Mapping] and/or will be captured in another BIRD, not here)

*Other Notes:* If a pin\_name in the component section does not have an entry under the [Pin Reference] keyword, and there is a model\_name on that pin that is not NC, POWER or GND, then the EDA tool must choose a reference node for simulation results at the pin\_name and rail terminals of the model. Some EDA tools use simulator Node 0 for this reference. Some EDA tools use the rail terminal that has a reference voltage [\* Reference] ([Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], [GND Clamp Reference], [Pullup Reference], and [External Reference]). The [Pin Reference] keyword allows the model maker to describe the node.

When analyzing the waveforms at the buffer to compare them to such things as Vinl, Vinh, Vmeas and Receiver Thresholds, the voltage at the I/O Pin relative to the EDA tool reference node, must be adjusted by the difference of the voltage at the [Pin Reference] pin\_name term relative to the EDA tool reference node and the value of the [\* Reference] for the corresponding bus\_label terminal.

Note that the “Reference\_supply” in the [Receiver Thresholds] section may not be the same rail bus\_label as the bus\_label in the [Pin Reference] for that buffer. The equation for the adjusted Vth must also supply this correction to the voltage at the Reference\_supply terminal relative to the EDA tool reference node.

Note, the appropriate reference supply should be a bus\_label terminal whose corresponding [\* Reference] value is based on the dominant internal electrical circuitry. For some technologies, the appropriate reference, such as PECL and Open\_source configurations, the appropriate reference should be the most positive terminal. For Bipolar (TTL) technology, the most negative terminal or the one that is closest to GND may be the appropriate value. For some technologies, the threshold values can depend on two rails. So the model developer should choose the one that would impact threshold and Vref and Vmeas values.

Normally the [Pin Reference] terminal is in a bus\_label that is supplied to one of the [\* Reference] terminals of the model, however there may be models that none of the [\* Reference] terminals of the model are used as the reference node of the test fixture. For example, this may occur on RS232, and PECL buffers where none the [\* Reference] voltages are 0.0 V relative to the test fixture reference. This may only occur if there is a pin with a signal\_name (note using signal\_name purposely here) that is used as the test fixture reference. By definition of the data derivation methods described in this document for Devices Under Test, this voltage is 0.0 V relative to the test fixture reference. In this case the voltage at the I/O Pin relative to the EDA tool reference node, must be adjusted by the voltage at the [Pin Reference] node (note the [Pin Reference] node is not a terminal of the model) relative to the EDA tool reference node.

*Example:*

[Component] Reference\_Node\_Example

| ...

|

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

|

1 IO\_CMOS\_3\_3 IO\_CMOS\_3\_3

2 IO\_CMOS\_3\_3-PC\_5\_0 IO\_CMOS\_3\_3-PC\_5\_0

3 IO\_OPEN\_SOURCE\_3\_3 IO\_OPEN\_SOURCE\_3\_3

4 IO\_TTL\_5\_0 IO\_TTL\_5\_0

|

5 IO\_ECL\_0\_0 IO\_ECL\_0\_0

6 IO\_PECL\_5\_0 IO\_PECL\_5\_0

7 IO\_PECL\_2\_0\_M3\_2 IO\_PECL\_2\_0-M3\_2

|

8 OUT\_RS232 OUT\_RS232\_10\_0-M10\_0

9 IN\_RS232\_5\_0 IN\_RS232\_5\_0

|

| Power Rail Voltages for Examples in [Pin Mapping]

|

20 VCC\_10\_0 POWER | 10.0 V

21 VCC\_5\_0 POWER | 5.0 V

22 VCC\_3\_3 POWER | 3.3 V

23 VCC\_2\_0 POWER | 2.0 V

24 VEE\_0\_0 GND | 0.0 V

25 VSS\_M3\_2 POWER | -3.2 V

26 VSS\_M5\_2 POWER | -5.2 V

27 VSS\_M10\_0 POWER | -10.0 V

|

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref

|

1 VEE\_0\_0 VCC\_3\_3 | IO\_CMOS\_3\_3

2 VEE\_0\_0 VCC\_3\_3 VEE\_0\_0 VCC\_5\_0 | IO\_CMOS\_3\_3-\_PC\_5\_0

|

3 VEE\_0\_0 VCC\_3\_3 VEE\_0\_0 VCC\_3\_3 | IO\_OPEN\_SOURCE\_3\_3

|

4 VEE\_0\_0 VCC\_5\_0 | IO\_TTL\_5\_0

|

5 VEE\_0\_0 VEE\_0\_0 VSS\_M5\_2 VEE\_0\_0 | IO\_ECL\_0\_0

6 VCC\_5\_0 VCC\_5\_0 VEE\_0\_0 VCC\_5\_0 | IO\_PECL\_5\_0

7 VCC\_2\_0 VCC\_2\_0 VSS\_M3\_2 VCC\_2\_0 | IO\_PECL\_2\_0-M3\_2

|

8 VSS\_M10\_0 VCC\_10\_0 | OUT\_RS232\_10\_0-M10\_0

9 VEE\_0\_0 VCC\_5\_0 | IN\_RS232\_5\_0

|

20 NC VCC\_10\_0 | POWER 10.0 V

21 NC VCC\_5\_0 | POWER 5.0 V

22 NC VCC\_3\_3 | POWER 3.3 V

23 NC VCC\_2\_0 | POWER 2.0 V

24 VEE\_0\_0 NC | GND 0.0 V

25 NC VSS\_M3\_2 | POWER -3.2 V

26 NC VSS\_M5\_2 | POWER -5.2 V

27 NC VSS\_M10\_0 | POWER -10.0 V

|

[Pin Reference] bus\_label

|

| For CMOS, the pulldown\_ref and pullup\_ref are equally dominant for thresholds

|

1 VEE\_0\_0 | VCC\_3\_3 could also be chosen

2 VEE\_0\_0 | VCC\_3\_3 could also be chosen

|

| For IO\_Open Source models the pullup\_ref entry is dominant for thresholds

|

3 VCC\_3\_3 | VCC\_3\_3 is the dominant reference

|

| For TTL, the pulldown\_ref is the dominant reference

|

4 VEE\_0\_0 | VEE\_0\_0 is the dominant reference

|

| For ECL/PECL, the most positive voltage (pullup\_ref = pulldown\_ref) is dominant

|

5 VEE\_0\_0

6 VCC\_5\_0

7 VCC\_2\_0

|

| For normal OUT\_ RS232 with +/- voltages generated by charge pumps, either

| the pulldown\_ref or the pullup\_ref are equally dominant

|

8 VSS\_M10\_0 | VCC\_10\_0 is equally dominant for RS232 Output

9 VEE\_0\_0 | VCC\_5\_0 is equally dominant for CMOS Input

|

**BACKGROUND INFORMATION/HISTORY:**

Walter Katz gave a presentation “Receiver\_Thresholds Assume GND=0.0V=Node 0” in the April 19, 2016 IBIS-ATM meeting, describing this issue.

Bob Ross gave a presentation "[Pin Reference] Cases regarding dominant internal electrical circuitry dependencies at the May 3, 2016 IBIS-ATM meeting that showed the pullup reference dominance for ECL/PECL, and showed that CMOS has equal dominance between pulldown and pullup references